

What is claimed is:

1 1. A method for fabricating a portion of a semiconductor
2 device comprising:

3 forming a gate structure on a substrate, the gate
4 structure including an insulating oxide layer, a nitride
5 layer and a polysilicon layer, wherein the oxide layer is
6 located on the substrate, the nitride layer is located on
7 the oxide layer, and the polysilicon layer is located on
8 the nitride layer; and

9 reoxidizing the gate structure to form a layer of
10 oxide over the gate structure.

1 2. The method of claim 1, wherein said forming step
2 comprises:

3 depositing the insulating oxide layer on the
4 substrate;

5 depositing the polysilicon layer on the oxide
6 layer;

7 implanting nitrogen ions into the layers; and

8 annealing the layers to form a nitride layer
9 between the oxide layer and the polysilicon layer.

1 3. The method of claim 2, wherein the implanting step
2 includes implanting nitrogen ions into the layers at a dose
3 from about $1E14$ ions/cm² to about $1E16$ ions/cm².

1 4. The method of claim 2, wherein the annealing step
2 includes annealing the layers in an inert ambient gas at a
3 temperature from about 800°C to about 1100°C.

1 5. The method of claim 2, wherein the annealing step
2 includes annealing the layers in an inert ambient gas at a
3 temperature from about 900°C to about 1200°C using a rapid
4 thermal process.

1 6. The method of claim 2, wherein the annealing step
2 includes annealing the layers for about 15 minutes to about
3 60 minutes.

1 7. The method of claim 2, wherein the annealing step
2 forms a nitride layer from about 10 Å to about 50 Å thick.

1 8. The method of claim 2, wherein the reoxidizing step
2 includes reoxidizing the gate structure to form an oxide
3 layer from about 25 Å to about 500 Å thick.

1 9. The method of claim 2, wherein prior to the
2 reoxidizing step, forming source and drain regions in the
3 substrate.

1 10. The method of claim 2, wherein the implanting step
2 includes implanting nitrogen ions into the layers at a
3 dose from about 1E14 ions/cm² to about 1E16 ions/cm².

1 11. The method of claim 10, wherein the annealing step
2 includes annealing the layers for about 15 minutes to about
3 60 minutes.

1 12. The method of claim 11, wherein the annealing step
2 further includes annealing the layers in an inert ambient
3 gas at a temperature from about 800°C to about 1100°C.

1 13. The method of claim 11, wherein the annealing step
2 further includes annealing the layers using rapid thermal
3 processing in an inert ambient gas at a temperature from
4 about 900°C to about 1200°C using a rapid thermal process.

1 14. The method of claim 13, wherein the inert ambient gas
2 is argon.

1 15. The method of claim 13, wherein the implanting step
2 includes implanting $^{15}\text{N}_2^+$ nitrogen ions.

1 16. The method of claim 15, wherein the reoxidizing step
2 includes reoxidizing the gate structure for form a oxide
3 layer from about 25 Å to about 500 Å thick.

1 17. The method of claim 1, wherein said forming step
2 comprises:

3 depositing the insulating oxide layer on the
4 substrate;

5 depositing the nitride layer on the oxide layer;

6 depositing the polysilicon layer on the nitride layer.

1 18. The method of claim 17, wherein the depositing step
2 includes depositing nitride layer on the insulating oxide
3 layer to a thickness from about 10 Å to about 50 Å.

1 19. The method of claim 17, wherein the reoxidizing step
2 includes reoxidizing the gate structure to form an oxide
3 layer from about 25 Å to about 500 Å thick.

1 20. The method of claim 17, wherein the step of forming a
2 gate structure further includes selectively etching away
3 portions of the insulating oxide, nitride, and polysilicon
4 layers to expose substrate and form a peripheral edge
5 around the gate structure; and

6 wherein the reoxidizing step comprises exposing the
7 substrate to an oxidizing ambient to oxidize the exposed
8 substrate.

1 21. The method of claim 20, wherein the exposing step
2 causes an uplift in a peripheral portion of the nitride
3 layer.

1 22. The method of claim 20, wherein the exposing step
2 causes an indentation in the substrate near a peripheral
3 edge of the gate structure.

1 23. The method of claim 17, wherein prior to the
2 reoxidizing step, forming source and drain regions in the
3 substrate.

FOOTNOTES

1 24. A method for fabricating a portion of a semiconductor
2 device comprising:

3 forming an oxide gate layer on a surface of a
4 substrate;

5 forming a nitride layer on the oxide gate layer;

6 forming a polysilicon layer on the nitride layer;

7 etching away the polysilicon and nitride layers in
8 selected areas to form a gate structure; and

9 reoxidizing the gate structure to form a layer of
10 oxide.

1 25. The method of claim 24, wherein the step of forming a
2 nitride layer comprises depositing a nitride layer on the
3 oxide gate layer.

1 26. The method of claim 24, wherein the step of forming a
2 nitride layer comprises forming a nitride layer of about 10
3 Å to about 50 Å thick on the oxide gate layer.

1 27. The method of claim 24, wherein the step of
2 reoxidizing the exposed substrate comprises reoxidizing the
3 reoxidizing the exposed substrate to form an oxide layer
4 from about 25 Å to about 500 Å thick.

1 28. The method of claim 24, wherein the step of etching
2 exposes the surface of the substrate; and

3 wherein the step of reoxidizing the exposed substrate
4 comprises exposing the substrate to an oxidizing ambient to
5 oxidize the exposed substrate surface.

1 29. The method of claim 28, wherein the exposing step
2 causes an uplift in a portion of the nitride layer
3 proximate to a peripheral edge of the gate structure.

1 30. The method of claim 28, wherein the exposing step
2 includes exposing the substrate to the oxidizing ambient at
3 a temperature from about 650°C to about 900°C.

1 31. The method of claim 29, wherein the exposing step
2 further includes exposing the substrate to the oxidizing
3 ambient for about 10 minutes to about 60 minutes.

1 32. The method of claim 24, wherein prior to the
2 reoxidizing step, forming source and drain regions in the
3 substrate.

1 33. The method of claim 24, further comprising forming
2 source and drain regions in the substrate after the
3 reoxidizing step.

1 34. A method for fabricating a portion of a semiconductor
2 device comprising:

3 forming an oxide layer on a substrate;

4 forming a polysilicon layer on the oxide layer;

5 implanting a nitrogen ion into the oxide and
6 polysilicon layers;

7 annealing the oxide and polysilicon layers to form a
8 nitride layer between the oxide and polysilicon layers;

9 etching the polysilicon, nitride, and oxide layers to
10 expose the substrate and form a gate structure; and

11 reoxidizing the exposed substrate and the gate
12 structure.

1 35. The method of claim 34, wherein the implanting step
2 includes implanting nitrogen ions into the layers at a dose
3 from about $1E14$ ions/cm² to about $1E16$ ions/cm².

1 36. The method of claim 34, wherein the implanting step
2 includes implanting $^{15}N_2^+$ nitrogen ions into the layers.

1 37. The method of claim 34, wherein the annealing step
2 further includes annealing the layers in an inert ambient
3 gas at a temperature from about 800°C to about 1100°C.

1 38. The method of claim 34, wherein the annealing step
2 further includes annealing the layers using rapid thermal
3 processing in an inert ambient gas at a temperature from
4 about 900°C to about 1200°C.

1 39. The method of claim 34, wherein the annealing step
2 includes annealing the layers for about 15 minutes to about
3 60 minutes.

1 40. The method of claim 34, wherein the annealing step
2 forms a nitride layer from about 10 Å to about 50 Å thick

1 41. The method of claim 34, wherein the etching step
2 further includes creating a peripheral edge around the gate
3 structure.

1 42. The method of claim 41, wherein the step of
2 reoxidizing the exposed substrate comprises exposing the
3 substrate to an oxidizing ambient to oxidize the exposed
4 substrate.

1 43. The method of claim 42, wherein the exposing step
2 causes an uplift in a portion of the nitride layer
3 proximate to the peripheral edge.

1 44. The method of claim 34, wherein prior to the
2 reoxidizing step, forming source and drain regions in the
3 substrate.

1 45. The method of claim 34, further comprising forming
2 source and drain regions in the substrate after the
3 reoxidizing step.

1 46. An integrated circuit device comprising:

2 a substrate;

3 a gate structure, wherein the gate structure includes:

4 a gate oxide layer on the substrate,

5 a nitride layer on the gate oxide layer, and

6 a polysilicon layer over the nitride layer;

7 a channel region under the gate structure; and

8 source/drain regions in the substrate adjacent the
9 channel region.

1 47. The integrated circuit device of claim 46, wherein the
2 nitride layer is from about 10 Å to about 50 Å thick.

1 48. The integrated circuit device of claim 46, wherein the
2 nitride layer is deposited over said gate oxide layer.

1 49. The integrated circuit device of claim 46, wherein the
2 nitride layer is formed by nitrogen implantation to form an
3 implanted area and by annealing of the implanted area.

1 50. The integrated circuit device of claim 46, wherein the
2 gate has a peripheral edge and further including an uplift
3 in the nitride layer occurring in portions of the nitride
4 layer proximate the peripheral edge of the gate structure,
5 the uplift caused by reoxidation of the gate structure,
6 wherein asperities are absent from the polysilicon layer.

1 51. The integrated circuit device of claim 46, wherein the
2 substrate has a surface and further including an
3 indentation in the surface of the substrate located
4 proximate to the peripheral edge of the gate, the
5 indentation resulting from reoxidation of the integrated
6 circuit device.

1 52. The integrated circuit device of claim 46 further
2 wherein the gate structure includes sidewall spacers
3 located on each edge of the gate structure and lightly
4 doped drain regions in the substrate located in the
5 substrate below the sidewall spacers.

1 53. The integrated circuit device of claim 46, wherein the
2 substrate is a p-type substrate and wherein the
3 source/drain regions are formed by implanting n-type
4 impurities in the p-type substrate.

1 54. The integrated circuit device of claim 53, wherein the
2 source/drain regions are implanted prior to reoxidation.

1 55. The integrated circuit device of claim 53, wherein the
2 source/drain regions are implanted after oxidation.